DMACONT PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - apps www.analog.com/MicroConverter

4 ;

5 ; Date : October 2003

6 ;

7 ; File : DMAcont.asm

8 ;

9 ; Description : performs continuous mode DMA conversions on a

10 ; single ADC channel at 104KSPS

11 ; Debugger or emulator must be used to view results.

12 ;

13 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

14

15 $MOD842 ; use 8052&ADuC842 predefined symbols

16

0040 17 DMACOUNT EQU 64 ; number of AD readings to take

0010 18 DMAINIT EQU 10h ; top nibble of DMAINIT = ADC channel

19

20 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

21 ; DEFINE VARIABLES IN INTERNAL RAM

---- 22 DSEG

0060 23 ORG 0060h

0060 24 DMASTOPH: DS 1 ; DMA stop address hi byte

0061 25 DMASTOPL: DS 1 ; DMA stop address lo byte

26

27 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

28 ; DEFINE SEGMENT OF EXTERNAL RAM

---- 29 XSEG

0000 30 ORG 000000h

0000 31 DMASTART: DS DMACOUNT\*2 ; location for DMA results

0080 32 DMASTOP: DS 4 ; location for DMA stop sequence

33

34 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

35 ; BEGINNING OF CODE

---- 36 CSEG

0000 37 ORG 0000h

0000 02004B 38 JMP MAIN ; jump to main program

39

40 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

41 ; INTERRUPT VECTOR SPACE

0033 42 ORG 0033h ; (ADC ISR)

0033 C2DD 43 CLR CCONV ; stop conversions

0035 C3 44 CLR C ; clear C to indicate DMA done

0036 32 45 RETI

46

47 ;====================================================================

48 ; MAIN PROGRAM

004B 49 ORG 004Bh

004B 50 MAIN:

51

52 ; PRECONFIGURE external RAM for DMA capture on a single channel...

004B 75EF00 53 MOV ADCCON1,#00h ; set MD1, MD0 TO 0

54

004E 900080 55 MOV DPTR,#DMASTOP ; store DMASTOP 16bit value..

0051 858261 56 MOV DMASTOPL,DPL ; ..as a high byte & low byte

0054 858360 57 MOV DMASTOPH,DPH ; (for use in GETSTOPFLAG subr)

0057 900000 58 MOV DPTR,#DMASTART ; set DPTR to DMASTART address

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005A 7410 59 SETUP: MOV A,#DMAINIT ; set up x-mem with init value

005C F0 60 MOVX @DPTR,A

005D A3 61 INC DPTR

005E E4 62 CLR A ; clear second byte

005F F0 63 MOVX @DPTR,A

0060 A3 64 INC DPTR

0061 12008B 65 CALL GETSTOPFLAG ; C cleared if DPTR>=DMAEND

0064 40F4 66 JC SETUP

67

0066 7410 68 MOV A,#DMAINIT ; "dummy" DMA location..

0068 F0 69 MOVX @DPTR,A ; ..to preceed stop command

0069 A3 70 INC DPTR

006A E4 71 CLR A

006B F0 72 MOVX @DPTR,A

006C A3 73 INC DPTR

74

006D 74F0 75 MOV A,#0F0h ; DMA stop command

006F F0 76 MOVX @DPTR,A

77

78 ; CONFIGURE ADC for DMA conversion...

79

0070 75D200 80 MOV DMAL,#0 ; start address for DMA operation

0073 75D300 81 MOV DMAH,#0 ; (must write DMA registers in this

0076 75D400 82 MOV DMAP,#0 ; order: DMAL, DMAH, DMAP)

83

0079 75D840 84 MOV ADCCON2,#040h ; enable DMA mode

007C 75EFAC 85 MOV ADCCON1,#0ACh ; 9.5us conv+acq time

86

007F D2AF 87 SETB EA ; enable interrupts

0081 D2AE 88 SETB EADC ; enable ADC interrupt

89

90 ; LAUNCH DMA conversion... when complete, ADC interrupt will clear C

91

0083 D2DD 92 SETB CCONV ; start continuous ADC conversions

0085 D3 93 SETB C

0086 40FE 94 JC $ ; wait for DMA to finish

95

0088 00 96 NOP ;.................................... SET BREAKPOINT HERE

97

98 ; REPEAT entire program...

99

0089 80C0 100 JMP MAIN

101

102 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

103 ; SUBROUTINE

104

008B 105 GETSTOPFLAG: ; clears C if DPTR>=DMASTOP

008B D3 106 SETB C

008C E583 107 MOV A,DPH

008E B56005 108 CJNE A,DMASTOPH,RET1 ; C cleared if DPH>=DMASTOPH

0091 E582 109 MOV A,DPL

0093 B56100 110 CJNE A,DMASTOPL,RET1 ; C cleared if DPL>=DMASTOPL

0096 22 111 RET1: RET

112

113 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

114

115 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

CCONV. . . . . . . . . . . . . . B ADDR 00DDH PREDEFINED

DMACOUNT . . . . . . . . . . . . NUMB 0040H

DMAH . . . . . . . . . . . . . . D ADDR 00D3H PREDEFINED

DMAINIT. . . . . . . . . . . . . NUMB 0010H

DMAL . . . . . . . . . . . . . . D ADDR 00D2H PREDEFINED

DMAP . . . . . . . . . . . . . . D ADDR 00D4H PREDEFINED

DMASTART . . . . . . . . . . . . X ADDR 0000H

DMASTOP. . . . . . . . . . . . . X ADDR 0080H

DMASTOPH . . . . . . . . . . . . D ADDR 0060H

DMASTOPL . . . . . . . . . . . . D ADDR 0061H

DPH. . . . . . . . . . . . . . . D ADDR 0083H PREDEFINED

DPL. . . . . . . . . . . . . . . D ADDR 0082H PREDEFINED

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

GETSTOPFLAG. . . . . . . . . . . C ADDR 008BH

MAIN . . . . . . . . . . . . . . C ADDR 004BH

RET1 . . . . . . . . . . . . . . C ADDR 0096H

SETUP. . . . . . . . . . . . . . C ADDR 005AH